CLAIMS

1. (Original) A test apparatus, comprising:

a test driver including a drive channel and an input/output channel; and

a test board including a package, the package having mounted thereon a plurality of chips;

where the drive channel connects to drive pins associated with each of the plurality of chips in parallel; and

where the input/output channel connects to input/output pins associated with each of the plurality of chips in parallel.

2. (Original) The test apparatus of claim 1 where while one of the semiconductor chips is being tested the drive and input/output pins of other semiconductor chips are held in a high impedance state.

3. (Original) The test apparatus of claim 2 where the semiconductor chips are tested sequentially.

4. (Original) The test apparatus of claim 1 where the drive pins includes control and address pins.

5. (Original) A method of testing a package mounted with a plurality of semiconductor chips, comprising:

connecting a drive channel of a test driver to a plurality of drive pins corresponding to the plurality of semiconductor chips;

connecting an input/output channel of a test driver to a plurality of input/output pins corresponding to the plurality of semiconductor chips; and

setting, while one of the semiconductor chips is being tested, the drive and input/output pins of other semiconductor chips to a high impedance state.

6. (Original) The method of claim 5 where the drive pins include control and address pins.